Remarks

Claims 1, 2, 3, 4 and 16 have been amended. Claim 25 has been added. Please charge any clam fees or any other fees for entry of this Amendment to our Deposit Account 03-3415.

The Examiner has rejected applicants' claims 1-7, 12, 13, 15-18 and 22 under 35 USC 103(a) as unpatentable over the Izumi, et al. patent (US Patent No. 6,160,673) taken in view of the Twitchell, et al. patent (US Patent No. 6,281,936) in further view of the Sasaki et al. patent (US Patent No. 5,774,290). Claims 8, 9 and 11 have been rejected under 35 USC 103(a) based on the latter patents taken with the Williams patent (US Patent No. 6,344,749). Finally, claim 14 has been rejected under 35 USC 103(a) based on the Izumi, et al., Twitchell, et al. and Sasaki et al. patents taken with the Limberg, et al. patent (US Patent No. 6,426,780). These rejections are respectfully traversed.

Applicants' independent claims 1 and 16 have been amended to better define applicants' invention. In particular, amended claim 1 recites a reproducing apparatus, comprising: reproducing means for reproducing an information signal from a recording medium; equalizing means for controlling a group delay of the information signal reproduced by said reproducing means; converting means for sampling the information signal output from said equalizing means and for converting the information signal into a digital signal composed of a plurality of bits per sample; detecting means for converting the digital signal output from said converting means into a n-values signal per sample; and control means for controlling said equalizing means by using both the digital signal to be input to said detecting means and the n-values signal output from said detecting means, wherein said control means includes multiplying means for multiplying the digital signal to be input to said detecting means by the n-values signal output from said detecting means to output an evaluation value signal representing a level of predetermined

frequency of the information signal output from said equalizing means, and wherein said control means controls a group delay characteristic of said equalizing means according to the evaluation value signal. Claim 16 has similar features and has been similarly amended.

Applicants' arguments set forth in the Response After Final Under 37 CFR § 1.116 filed August 6, 2007 are herein restated and incorporated by reference. Applicant submits that these arguments demonstrate that applicants' claims patentably distinguish over the cited references. In response to these arguments, the Examiner in the Advisory Action states as follows:

> "Applicants' arguments filed June 5, 2007 have been fully considered but they are not persuasive. On pages 3-5 applicant argues that Izumi et al in view of Twitchell et al in view of Sasaki et al does teach, suggest or fairly disclose 'converting means for sampling the information signal output from said equalizing means and for converting the information signal into a digital [signal] composed of a plurality of bits per sample.' It is stated in Twitchell et al that a conversion and equalization of the signal occurs as seen in Figure 1 and further described in Column 3 Lines 15-42 and furthermore in Column 3 Lines 60+ through Column 4 Lines 1-32.
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> "Additionally, applicant argues the cited references fails to teach, disclose or suggest, 'detecting means for converting the digital signal output from said converting means into a n-values signal per sample.' Izumi et al disclose a detecting means as seen in Figure 1 and described in Column 11 Lines 38-48; however, fails to disclose the converting into n-values signal per sample. Sasaki et al teaches the system to convert the digital signal into n-values signal per sample as described in Column 3 Lines 50+ through Column 4 Lines 1-30.
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> "Applicant additionally argues that the cited references fail to teach 'control means for controlling a group delay characteristic of said equalizing means by using the digital signal to be input to said detecting means and a the n-values signal output from said detecting means' as recited in claim 1. Twitchell et al teaches the system equalizing the digital signal through detecting the values from sampling as described in Column 5 Lines 49+ through Column 6 Lines 1-24. The system provides sampling for detection and control of the signal. Although, all applicants points are understood the examiner can not agree and therefore the rejection is maintained."

In reviewing the above, it is not evident to applicant that "all applicants points" are understood by the Examiner as the Examiner has stated.

With respect to the Examiner's first point in which the Examiner cites Column 3, lines 15-42 and Column 3, lines 60+ through column 4, lines 1-32, of the Twitchell, et al. patent, in reviewing these passage they do not appear to mention "converting means for sampling the information signal output from said equalizing means and for converting the information signal into a digital signal composed of a plurality of bits per sample." In the first passage, there is no mention whatsoever of anything for performing such a conversion. In the second passage, a DAC 24, which follows the linear equalizer 46, is mentioned, but the "DAC 24 converts the information signal to an analog form." (Column 3, lines 61-62). So these passages do not teach "converting means for sampling the information signal output from said equalizing means and for converting the information signal into a digital signal composed of a plurality of bits per sample."

The Examiner then cites Column 11, lines 38-48, of the Izumi, et al. patent as disclosing a detecting means and Column 3, lines 50+ through Column 4, lines 1-30, of the Sasaki, et al. patent as disclosing a system to convert a digital signal into a n-values signal per sample to meet applicants' claimed feature of "detecting means for converting the digital signal output from said converting means into a n-values signal per sample." While the Izumi, et al. patent discloses in these lines the detection circuit 11, this circuit follows a fixed waveform equalizing circuit 4 and converts the waveform from the circuit 4 into a binary format, but the converted signal is not otherwise used to control the equalizer. Similarly, the passage of the Sasaki, et al. patent discloses an A/D converter 6 which converts the signal from the equalizer 5 into a digital signal having a plurality of bits per sample and which signal is restored to a two-level signal by a

Verterbi decoding circuit, but again neither the digital signal from the A/D converter nor the two-level signal from the Verterbi decoding circuit is used to control the equalizer 5.

Finally, the Examiner cites Column 5, line 49+ through Column 6, lines 1-24, of the Twitchell, et al. patent as teaching a "control means for controlling a group delay characteristic of said equalizing means by using the digital signal to be input to said detecting means and a the n-values signal output from said detecting means." These lines of the Twitchell, et al. patent mention the series arrangement of linear equalizer 42, non-linear corrector 44 and linear equalizer 46 used to provide pre-distortion to correct the distortion of the power amplifier 20. There is no mention in this description of controlling each of these components by using the digital signal to be input to a detecting means and an n-value signal output from the detecting means, where the detecting means converts the digital signal from a converting means to a n-values per sample signal and where the converting means samples the signal from the component (equalizer) and converts it into a digital signal composed of a plurality of bits per sample.

In point of fact, all the signals through the components 48, 42, 50, 44, 52 and 46 in the Twitchell, et al. patent are part of the 8VSB exciter which processes information digitally. (Column 3, lines 46-47). Hence, there is no need or use of a converter for converter the output of the component to a digital signal. Moreover, the characteristics of the components 42, 44 and 46 are based on input digital signals to each component sampled and fed to the respective memories W, D and X and the signal fed to the memory Y, not based on the input to and output from such a converter.

Based on all of the above, applicant does not appreciate how the Examiner can combine the teachings of the references to arrive at the above-mentioned combination of features of applicants' converting means, detecting means and control means. Having said that applicants'

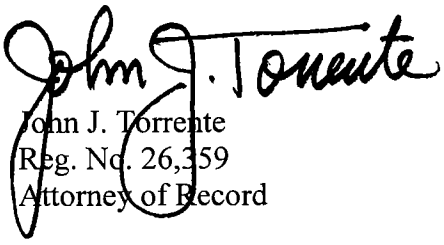
have nonetheless further clarified applicants' claims by further defining the control means as including multiplying means for multiplying the digital signal to be input to said detecting means by the n-values signal output from said detecting means to output an evaluation value signal representing a level of predetermined frequency of the information signal output from said equalizing means, and as controlling a group delay characteristic of said equalizing means according to the evaluation value. Applicants' note in this regard that the structure disclosed in FIG. 6 of the of the Izumi, et al. patent, while it shows multipliers, is the structure for the amplitude equalizer 6 and, thus, does not teach multiplying the digital signal to be input to said detecting means by the n-values signal output from said detecting means to output an evaluation value signal representing a level of predetermined frequency of the information signal output from said equalizing means.

This additional recitation thus further patentably distinguishes applicants' claims over the cited Izumi, et al., Twitchell, et al. and Sasaki, et al. patents. Moreover, the Williams patent and the Limberg, et al. patent fail to add anything to these patents to change this conclusion.

In view of the above, it is submitted that applicants' claims, as amended, patentably distinguish over the cited art of record. Accordingly, reconsideration of the claims is respectfully requested.

Dated: October 5, 2007

Respectfully submitted,



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